

## **Renesas Technology Develops “SiP Top-Down (Predictive) Design Environment” That Halves SiP Design Time**

— Improves design quality and cuts design time by half by enabling verification at the initial stage of aspects that significantly affect SiP design time, such as signal integrity and heat dispersion —

Tokyo, June 22, 2009 — Renesas Technology Corp. today announced the development of the SiP Top-Down Design Environment to boost efficiency when developing system in a package (SiP) products combining multiple chips, such as system on a chip (SoC) devices, MCUs, and memories, in a single package. It uses a top-down (predictive) design approach in which key characteristics, such as design quality and heat dispersion, are verified during the initial design stage.

The SiP Top-Down Design Environment integrates and optimizes a variety of tools, including a database of information on chips that can be incorporated in SiP products and a substrate layout tool. It provides a common user interface that enables transfer of data between design tools, enhancing their ease of use and flexibility, and delivers a design environment that automates tasks such as analysis during circuit simulations. These advances allow steps that have a big impact on the amount of time required to develop a new SiP, such as analysis of electrical characteristics to ensure signal integrity and thermal analysis of heat dispersion characteristics, to be implemented during the initial design stage. Design quality is enhanced while development time is cut in half.

### **< Product Background >**

Since an SiP combines in a single package multiple chips, such as SoCs, MCUs, and memories, the design of the package substrate configuration and wiring are more complex than is the case for a single-chip SoC device. In addition, ensuring signal integrity between the chips in an SiP is essential due to increased memory speed and capacity, and ensuring adequate heat dispersion is key because of the higher power consumption and heat generation density accompanying increased speed. These two factors have become very important aspects of SiP design. As a result, to achieve quicker SiP development it is critical to ensure signal integrity and also to make verification of heat dispersion performance as efficient as possible.

Previously, Renesas Technology used a project system to identify issues and countermeasures in order to increase design efficiency and reduce production cost for SiP products. This achieved a shortening of the time needed for package substrate design and helped cut costs associated with substrate production and SiP testing. The newly developed SiP Top-Down Design Environment meets the need for an approach that boosts SiP design quality while reducing development time. It replaces the conventional back annotation (analytical) design methodology, in which characteristics such as signal integrity and heat dispersion are analyzed at a late stage of the SiP design process, after the package substrate design has been completed, with a top-down design methodology, in which verification of a variety of characteristics is done in the initial SiP design stage. It employs an integrated design database and common user interface to enable automated analysis and other tasks as part of circuit simulation.

### **< Product Features >**

The main features of the SiP Top-Down Design Environment are described below.

- (1) Integrated design database and common user interface for multiple tools

In an SiP in which multiple chips are arranged in a stack, the chips and the package substrate are connected by wires made of gold or some other material. In the past, the analysis of electrical and thermal characteristics was independent of the wire bonding design and package substrate wiring design processes. As a result, it was necessary to update the substrate data manually for each tool used in chip and wiring analysis.

The new design environment uses an integrated design database to provide unified management of design data and easy connections for analysis of electrical or heat dissipation characteristics. Thus, data on chip shapes and positions as well as chip-to-chip connection data can be extracted from the database and connected to the substrate layout tool. In turn, wire bonding and substrate pattern data from the substrate layout tool can be connected to other analysis tools. For enhanced ease of use, a common interface is provided for running the tools and making settings.

(2) Noise analysis of large-scale package substrates at the initial design stage

Previously, analysis of the electrical characteristics of a large-scale package substrate involved division of the area to be analyzed into several sub-areas in order to complete the analysis in a practical amount of time. Since the manner in which the area to be analyzed is divided can affect the accuracy of the analysis, careful consideration had to be given to the division method itself. The circuit simulations also involved complex combinations of analysis conditions, such as SoC drive adjustment. As a result, building the simulation environment and determining the execution results was a very time consuming process, and it was difficult to estimate noise characteristics at the initial design stage.

The new design environment includes an electromagnetic field analysis tool that supports large-scale substrates. This means it is not necessary to divide up the area to be analyzed. In addition, simulation condition setting and result determination for circuit simulations are automated. It is therefore possible to estimate noise at the initial design stage based on the electrical characteristics.

(3) Heat dispersion analysis taking substrate layout into account

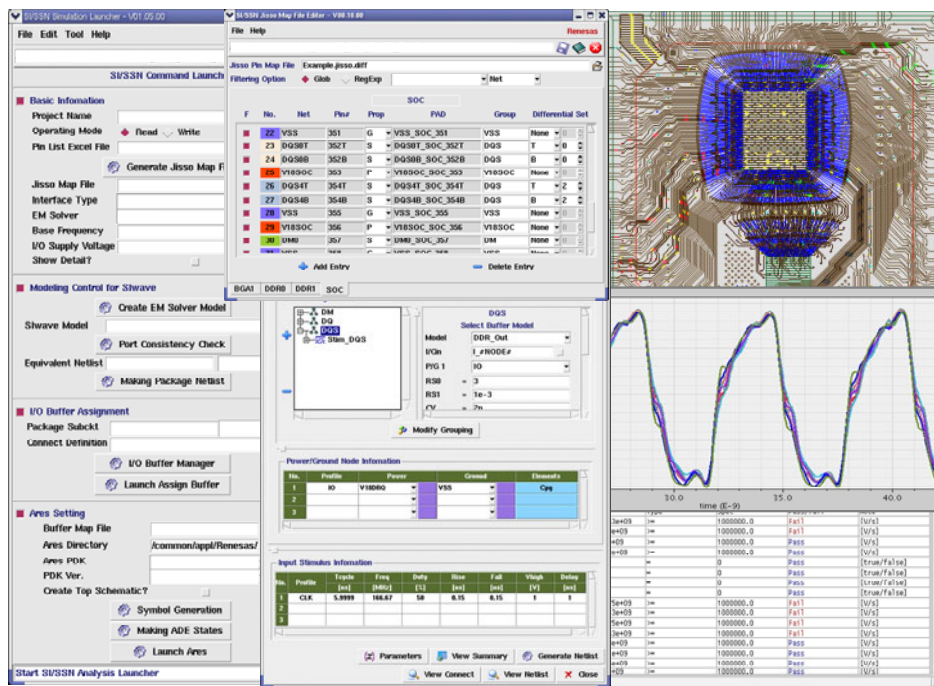
Previously, package models for evaluation of heat dispersion characteristics were created manually by referring to the substrate layout data. As a result, the development of package models for heat dispersion evaluation was time consuming and there were limits on the accuracy of the resulting models.

The new design environment extracts from the substrate layout data information on the conductor pattern area share (copper ratio), layer thickness, and materials of the internal SiP package wiring, power plane, etc., the number of via holes between layers, and the shapes and positions of the chips, and it automatically builds an environment for the heat dispersion evaluation package model. Another newly developed function applies the power consumption distribution of the SoC to the thermal analysis model so that the distribution of heat generation within the chips is taken into account. These advances not only increase the accuracy of the models, they make it possible to complete the thermal analysis in a short amount of time.

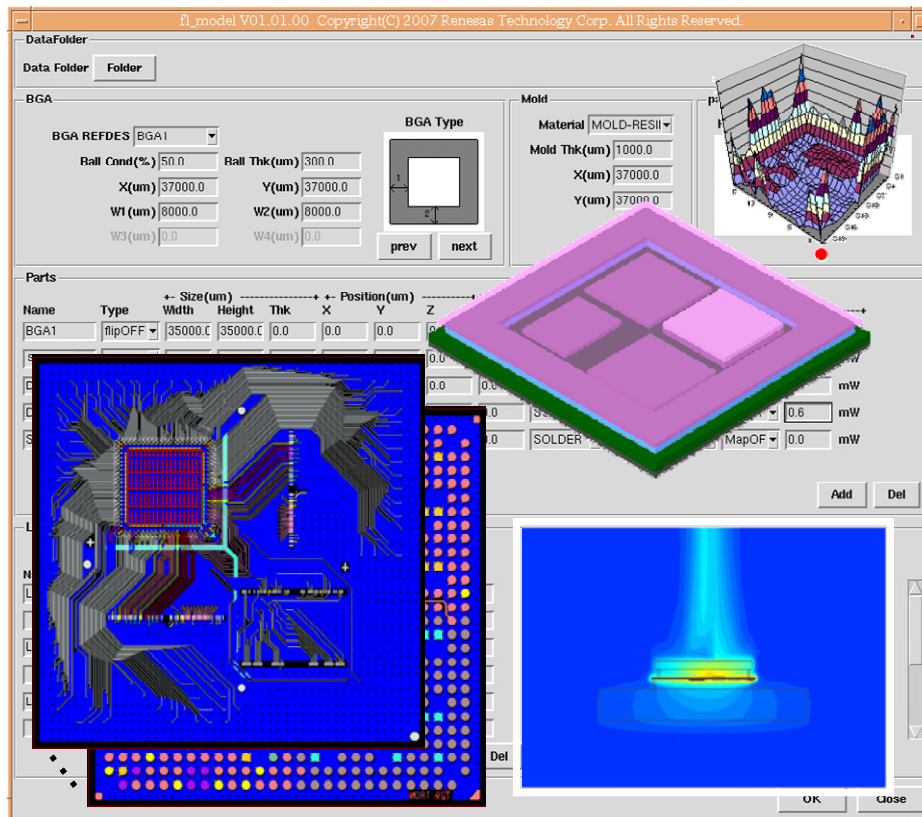
Renesas Technology plans to expand the application of the SiP Top-Down Design Environment to the development of broad range of SiP products and will continue to build development solutions that respond to evolving customer requirements.

# Supplementary figures

## 1. Example of large-scale noise analysis



## 2. Example of heat dispersion analysis taking substrate layout into account



\*\*\* Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice. \*\*\*