

Renesas Technology Introduces Highest Level Performance 72-Mbit QDR™ II+ SRAM and DDR II+ SRAM Family

— 533 MHz frequency for Next-Generation Communication Networks —

Tokyo, July 7, 2009 - Renesas Technology Corp. today announced the 72-Mbit Quad Data Rate II+ (QDR™ II+) and Double Data Rate II+ (DDR II+) high-speed SRAM*¹ product family for use in high-end routers and switches in next-generation communication networks. These SRAM products achieve the industry's fastest level operating speed and are compliant with the QDR Consortium*² industry standard. Additionally, this release also includes 72-Mbit QDR II and DDR II SRAM devices. The full range of devices, consisting of multiple speeds and configurations, will be available from August 2009 sequentially in Japan.

These new products offer the following features.

- (1) Achievement of the industry's fastest level operating speeds: 533 MHz for the QDR II+ and DDR II+ SRAM and 333 MHz for the QDR II and DDR II versions

For these products, Renesas greatly increased the operating speeds while maintaining low-voltage operation by utilizing the advanced 45 nm fabrication process. The QDR II SRAM products achieve the industry's highest operating speed level of 333 MHz, and the QDR II+ SRAM products also provide the industry's highest operating speed level of 533 MHz. These devices can support high-speed processing for packet look-up and packet buffer applications in high-end routers and switches that support 10G, 40G, and beyond multi-layer communication systems.

- (2) Broad portfolio of 72-Mbit devices

Renesas will provide products that support three data I/O widths (9, 18, or 36 bits) and two burst lengths (2 or 4 words). In addition, Renesas will also provide products that feature a built-in ODT (on-die termination) function that significantly reduces the signal quality degradation that can occur during high-speed operation. Renesas' extensive lineup of QDR II, DDR II, QDR II+, and DDR II+ SRAM products allows users to select solutions that are optimal for their systems.

< Product Background >

With the ever-growing popularity of the Internet, transmission speeds and the amount of traffic being sent to communication equipment continue to increase, with data rate speeds now exceeding 40-Gbits/second. Checking data destinations and managing data packet traffic in high-end networking equipment is driving the demand for high-density memory capable of high speeds. Furthermore, the complexity of data continues to increase with video, voice, and data applications, requiring even larger memory capacities.

Renesas Technology currently provides a broad range of SRAMs for industrial applications and for cache memory in UNIX*³ servers and workstations, and 18-Mbit Network SRAM and 36-Mbit DDR II and QDR II SRAM for communication equipment. As network equipment evolve to higher levels of performance and capability, Renesas Technology has leveraged its design expertise and manufacturing technologies to achieve higher speeds and high reliability for the 72-Mbit QDR II and QDR II+ SRAM products to meet the demands for higher speed, larger capacity, and greater bit widths required for communication applications.

< Product Details >

These products are available in all combinations of burst lengths and bit widths, and the standard HSTL (High-Speed Transistor Logic) interface is used for ultra high-speed synchronous SRAM.

The package used is a 165-pin plastic FBGA with a 15 mm × 17 mm size that features excellent thermal dissipation characteristics and is suitable for high-density mounting. These products are RoHS Directive*⁴ compliant and lead-free versions are also available. The QDR pin configuration can support seamless migration to densities up to 288 Mbits in the future. In addition, FBGA package products support the IEEE standard test access port and boundary scan architecture (IEEE Std 1149.1-1990) that allow interchange connection checking during module mounting to be conducted at the board level.

In future developments in this area, Renesas has a solid roadmap and commitment to develop even larger and higher performance QDR/DDR SRAM products to support evolving customer needs.

< Notes >

Notes: 1.

Quad Data Rate II+ (QDRTMII+) and Double Data Rate II+ (DDRII+) SRAM:

QDRII+ SRAM is an even faster version of the second generation QDR SRAM product. DDRII+ SRAM is also a faster version of the second generation DDR SRAM product.

QDR SRAM and DDR SRAM adopt a DDR technique where, while acquiring the address and control signals from the processor or controller in synchronization with the system clock, the SRAM also writes or reads data signals in synchronization with both the system clock and an inverted system clock signal. As a result, these devices can achieve transfer rates that are twice those of earlier synchronous SRAM. Furthermore, since the input and output pins are separate and isolated, read and write operations can be performed at the same time. This allows data to be transferred with excellent efficiency and makes it possible to achieve data rates that are four times those of earlier synchronous SRAM devices.

- Quad Data Rate and QDR include a new family of products developed by Cypress Semiconductor Corp., Integrated Device Technology, Inc., NEC Electronics Corporation, Samsung Electronics Co., Ltd., and Renesas Technology Corp.

2. The QDR Consortium (the QDR Co-Development Team):

In 1999, the QDR co-development team was created to define a new family of SRAM architectures for high-performance communications applications. The QDR co-development team currently consists of Cypress Semiconductor Corp., Integrated Device Technology, Inc., NEC Electronics Corporation, Samsung Electronics Co., Ltd., and Renesas Technology Corp. These companies cooperate in the development of the QDR family of networking SRAMs. They design and manufacture this family of products in their own fabrication facilities and develop products according to their own schedules, competing in the marketplace.

<http://www.qdrconsortium.com/>

3. UNIX is a registered trademark of The Open Group in the U.S. and other countries.
4. RoHS Directive: A European Union (EU) Directive for "the restriction of the use of certain hazardous substances in electrical and electronic equipment." It went into effect on July 1, 2006, and covers six substances: lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyl (PBB), and polybrominated diphenyl ether (PBDE).

* Other product names, company names, or brands mentioned are the property of their respective owners.

< Typical Applications >

- Next-generation communication equipment such as high-end routers and switches

< Specifications >

(1) 72-Mbit QDRII and QDRII+ SRAM

Product name	Non ODT	R1Q2A72**RBG* ¹	R1Q3A72**RBG* ¹	R1QGA72**RBG* ¹	R1QAA72**RBG* ¹
	ODT	-	-	R1QKA72**RBG* ¹	R1QDA72**RBG* ¹
Capacity	72 Mbits				
Type	QDRII			QDRII+	
Bit configuration	× 9/18/36 bit			× 9/18/36 bit	
Functions	2-word burst (separate I/O)		4-word burst (separate I/O)	4-word burst (separate I/O)	
Power supply voltage	Vdd	1.8 V ±0.1V			
	Vddq	1.4 V to Vdd		1.5 V ±0.1V	
Interface	HSTL				
Maximum operating frequency (MHz)	275		333	450	533
Minimum cycle time (ns)	3.6		3.0	2.2	1.9
Read latency (cycle)	1.5			2.0	2.5
JTAG* ²	Limited function of IEEE 1149.1				
Package	165-pin FBGA (15 × 17 mm) < lead-free versions are also available >				

(2) 72-Mbit DDRII SRAM

Product name	Non ODT	R1Q4A72**RBG* ¹	R1Q5A72**RBG* ¹	R1Q6A72**RBG* ¹
Capacity		72 Mbits		
Type		DDRII		
Bit configuration		× 9/18/36 bit		
Functions		2-word burst (common I/O)	4-word burst (common I/O)	2-word burst (separate I/O)
Power supply voltage	Vdd	1.8 V ±0.1V		
	Vddq	1.4 V to Vdd		
Interface		HSTL		
Maximum operating frequency (MHz)		333		
Minimum cycle time (ns)		3.0		
Read latency (cycle)		1.5		
JTAG* ²		Limited function of IEEE 1149.1		
Package		165-pin FBGA (15 × 17 mm) < lead-free versions are also available >		

(3) 72-Mbit DDRII+ SRAM

Product name	Non ODT	R1QHA72**RBG* ¹	R1QBA72**RBG* ¹	R1QJA72**RBG* ¹	R1QCA72**RBG* ¹
	ODT	R1QLA72**RBG* ¹	R1QEA72**RBG* ¹	R1QMA72**RBG* ¹	R1QFA72**RBG* ¹
Capacity		72 Mbits			
Type		DDRII+			
Bit configuration		× 9/18/36 bit			
Functions		2-word burst (common I/O)		4-word burst (common I/O)	
Power supply voltage	Vdd	1.8 V ±0.1V			
	Vddq	1.5 V ±0.1V			
Interface		HSTL			
Maximum operating frequency (MHz)		450	533	450	533
Minimum cycle time (ns)		2.2	1.9	2.2	1.9
Read latency (cycle)		2.0	2.5	2.0	2.5
JTAG* ²		Limited function of IEEE 1149.1			
Package		165-pin FBGA (15 × 17 mm) < lead-free versions are also available >			

Note 1. The ** is replaced by the bit structure to form the product name.

Example -- R1Q2A72**RBG: For a ×9 bit structure, the product name is R1Q2A7209RBG; for a ×18 bit structure, it is R1Q2A7218RBG; and for a ×36 bit structure, it is R1Q2A7236RBG.

Note 2. JTAG (Joint Test Action Group): Boundary scan test standard stipulated by IEEE 1149.1.

-###-

*** Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice. ***